MVME332XT
Intelligent Communications Controller User's Manual

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MOTOROLA

MVME332XT
Intelligent Communications Controller
User's Manual

(MVME332XT/D2)

NOTICE

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PREFACE

This manual provides general information, hardware preparation, installation instructions, and functional description for the MVME332XT Intelligent Communications Controller.

This manual is intended for anyone who wants to design OEM systems, supply additional capability to an existing compatible system, or in a lab environment for experimental purposes.

A basic knowledge of computers, and digital logic is assumed.

To use this manual, you should be familiar with the publications listed in the *Related Documentation* paragraph in Chapter 1 of this manual.

WARNING

THIS EQUIPMENT GENERATES, USES, AND CAN RADIATE RADIO FREQUENCY ENERGY AND IF NOT INSTALLED AND USED IN ACCORDANCE WITH THE INSTRUCTIONS MANUAL, MAY CAUSE INTERFERENCE TO RADIO COMMUNICATIONS. IT HAS BEEN TESTED AND FOUND TO COMPLY WITH THE LIMITS FOR A CLASS A COMPUTING DEVICE PURSUANT TO SUBPART J OF PART 15 OF FCC RULES, WHICH ARE DESIGNED TO PROVIDE REASONABLE PROTECTION AGAINST SUCH INTERFERENCE WHEN OPERATED IN A COMMERCIAL ENVIRONMENT. OPERATION OF THIS EQUIPMENT IN A RESIDENTIAL AREA IS LIKELY TO CAUSE INTERFERENCE IN WHICH CASE THE USER, AT HIS OWN EXPENSE, WILL BE REQUIRED TO TAKE WHATEVER MEASURES NECESSARY TO CORRECT THE INTERFERENCE.

SAFETY SUMMARY
SAFETY DEPENDS ON YOU

The following general safety precautions must be observed during all phases of operation, service, and repair of this equipment. Failure to comply with these precautions or with specific warnings elsewhere in this manual violates safety standards of design, manufacture, and intended use of the equipment. Motorola Inc. assumes no liability for the customer's failure to comply with these requirements. The safety precautions listed below represent warnings of certain dangers of which we are aware. You, as the user of the product, should follow these warnings and all other safety precautions necessary for the safe operation of the equipment in your operating environment.

GROUND THE INSTRUMENT.

To minimize shock hazard, the equipment chassis and enclosure must be connected to an electrical ground. The equipment is supplied with a three-conductor ac power cable. The power cable must either be plugged into an approved three-contact electrical outlet or used with a three-contact to two-contact adapter, with the grounding wire (green) firmly connected to an electrical ground (safety ground) at the power outlet. The power jack and mating plug of the power cable meet International Electrotechnical Commission (IEC) safety standards.

DO NOT OPERATE IN AN EXPLOSIVE ATMOSPHERE.

Do not operate the equipment in the presence of flammable gases or fumes. Operation of any electrical equipment in such an environment constitutes a definite safety hazard.

KEEP AWAY FROM LIVE CIRCUITS.

Operating personnel must not remove equipment covers. Only Factory Authorized Service Personnel or other qualified maintenance personnel may remove equipment covers for internal subassembly or component replacement or any internal adjustment. Do not replace components with power cable connected. Under certain conditions, dangerous voltages may exist even with the power cable removed. To avoid injuries, always disconnect power and discharge circuits before touching them.

DO NOT SERVICE OR ADJUST ALONE.

Do not attempt internal service or adjustment unless another person, capable of rendering first aid and resuscitation, is present.

USE CAUTION WHEN EXPOSING OR HANDLING THE CRT.

Breakage of the Cathode-Ray Tube (CRT) causes a high-velocity scattering of glass fragments (implosion). To prevent CRT implosion, avoid rough handling or jarring of the equipment. Handling of the CRT should be done only by qualified maintenance personnel using approved safety mask and gloves.

DO NOT SUBSTITUTE PARTS OR MODIFY EQUIPMENT.

Because of the danger of introducing additional hazards, do not install substitute parts or perform any unauthorized modification of the equipment. Contact your local Motorola representative for service and repair to ensure that safety features are maintained.

DANGEROUS PROCEDURE WARNINGS.

Warnings, such as the example below, precede potentially dangerous procedures throughout this manual. Instructions contained in the warnings must be followed. You should also employ all other safety precautions which you deem necessary for the operation of the equipment in your operating environment.

WARNING

**Dangerous voltages, capable of causing death, are present in this equipment.
Use extreme caution when handling, testing, and adjusting.**

(3/91)

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CHAPTER 1
GENERAL INFORMATION

Introduction

This manual provides general information, preparation for use, installation instructions, operating instructions, and functional description for the MVME332XT Intelligent Communications Controller. Unless otherwise specified, this module is referred to as the MVME332XT throughout the contents of this manual.

Features

The features of the MVME332XT include:

- 12.5 MHz MC68010 based Intelligent Peripheral Controller architecture.
- Firmware executes from no wait state 512K EPROMs.
- Firmware character buffering routines utilize no wait state 196K byte local and 64K byte dual ported RAM spaces for high performance.
- Eight asynchronous serial I/O channels support up to 38,400 baud, full-duplex operation with either hardware or software handshaking (all eight ports are EIA-232-D compatible).
- Modem and terminal interface selection made via jumper arrays on the MVME710/MVME710A Eight Channel Serial I/O Distribution Module.
- One Centronics compatible parallel printer port supported (accessible via a shielded front panel mounted connector).
- MVME332XT firmware supports output character processing for line printer I/O.
- VMEbus requester is Release-On-Request design that supports early release of BBSY* (may be configured for fairness mode operation to reduce bus starvation problems in heavily loaded VME systems.
- VMEbus master and slave interfaces are A32/A24, D16.

Specifications

The specifications for the MVME332XT are given in Table 1-1.

Table 1-1. MVME332XT Specifications

Characteristics	Specifications
Power requirements	+5 Vdc @ 4.7 A maximum (4.2 A typical) +12 Vdc @ 100 mA maximum (50mA typical) -12 Vdc @ 100 mA maximum (50 mA typical)
Operating temperature	0° to 55° C at point of entry of forced air
Storage temperature	-40° to 85° C
Relative humidity	5% to 90% (non-condensing)
Physical characteristics	(excluding front panel)
Height Depth Thickness	9.187 inches (233.35 mm) 6.299 inches (160.00 mm) 0.063 inches (1.6 mm)

FCC Compliance

This VMEmodule (MVME332XT) was tested in an FCC-compliant chassis, and meets the requirements for Class A equipment. FCC compliance was achieved under the following conditions:

1. Shielded cables on all external I/O ports.
2. Cable shields connected to earth ground via metal shell connectors bonded to a conductive module front panel.
3. Conductive chassis rails connected to earth ground. This provides the path for connecting shields to earth ground.
4. Front panels screws properly tightened.

For minimum RF emissions, it is essential that the conditions above be implemented; failure to do so could compromise the FCC compliance of the equipment containing the modules.

General Description

The MVME332XT is an intelligent VMEmodule that provides a universal interface between VME systems and asynchronous serial I/O peripheral devices, such as EIA-232-D modems and terminals. The MVME332XT contains a 12.5MHz MC68010 microprocessor that controls four MK68564 Serial I/O Controller devices and relieves the system host processor from serial communication controlling tasks. The MVME332XT supports eight asynchronous serial communication channels at a maximum simultaneous speed of 38,400 baud full duplex.

Related Documentation

The following publications are applicable to the MVME332XT and may provide additional helpful information. If not shipped with this product, they may be purchased from Motorola, Inc, Technical Literature Center, 1919 West Fairmont Drive, Suite 8, Tempe, AZ 85282; Telephone 1-800-458-6443; FAX (602) 438-0240. Non-Motorola documents may be obtained from the sources listed.

Document Title	Motorola Publication Number
MVME710 Eight Channel Serial I/O Distribution Module User's Mamual	MVME710
or	
MVME710A Eight Channel Serial I/O Distribution Module User's Mamual	MVME710A
MC68000 8-/16-/32-Bit Microprocessor User's Manual	MC68000UM
MC68230 Parallel Interface/Timer Data Sheet	MC68230/D
MVME332XT Intelligent Communications Controller Support Information (Refer to the *Support Information* section in this chapter)	SIMVME332XT

NOTE: Although not shown in the above list, each Motorola Computer Group manual publication number is suffixed with characters which represent the revision level of the document, such as /D2 (the second revision of a manual); each supplement bears the same number as the manual but has a suffix such as /A1 (the first supplement to the manual).

The following publications are available from the sources indicated.

ANSI/IEEE Std 1014-1987 Versatile Backplane Bus: The Institute of Electrical and Electronics Engineers, Inc., 345 East 47th Street, New York, NY 10017, USA. (VMEbus specification)

Support Information

The SIMVME332XT manual contains the connector interconnect signal information, parts list, and the schematics for the MVME332XT.

This manual may be obtained free of charge from Motorola, Inc, Computer Group Technical Literature Center, 1919 West Fairmont Drive, Suite 8, Tempe, AZ 85282; Telephone 1-800-458-6443; FAX (602) 438-0240.

Manual Terminology

Throughout this manual, a convention has been maintained whereby data and address parameters are preceded by a character which specifies the numeric format as follows:

$	dollar	specifies a hexadecimal number
%	percent	specifies a binary number
&	ampersand	specifies a decimal number

Unless otherwise specified, all address references are in hexadecimal throughout this manual.

An asterisk (*) following the signal name for signals which are level significant denotes that the signal is true or valid when the signal is low.

An asterisk (*) following the signal name for signals which are edge significant denotes that the actions initiated by that signal occur on high to low transition.

In this manual, assertion and negation are used to specify forcing a signal to a particular state. In particular, assertion and assert refer to a signal that is active or true; negation and negate indicate a signal that is inactive or false. These terms are used independently of the voltage level (high or low) that they represent.

CHAPTER 2
HARDWARE PREPARATION AND INSTALLATION

Introduction

This chapter provides unpacking instructions, hardware preparation, and installation instructions for the MVME332XT.

Unpacking Instructions

NOTE

If the carton is damaged upon receipt, request carrier's agent be present during unpacking/ inspection of equipment.

Unpack equipment from shipping carton. Refer to packing list and verify that all items are present. Save packing material for storing and reshipping of equipment.

Hardware Preparation

To select the desired configuration and ensure proper operation of the MVME332XT, certain modifications may be made before installation. These changes are made through jumper arrangements on the headers. The location of the headers, switches, LEDs, and connectors on the MVME332XT is illustrated in Figure 2-1. The module has been factory tested and is shipped with factory-installed jumper configurations that are described in the following sections with each header description. The module is operational with factory-installed jumper configurations. The module is configured to provide the functions required for a VMEbus system. It is necessary to make changes in the jumper arrangements for the following conditions:

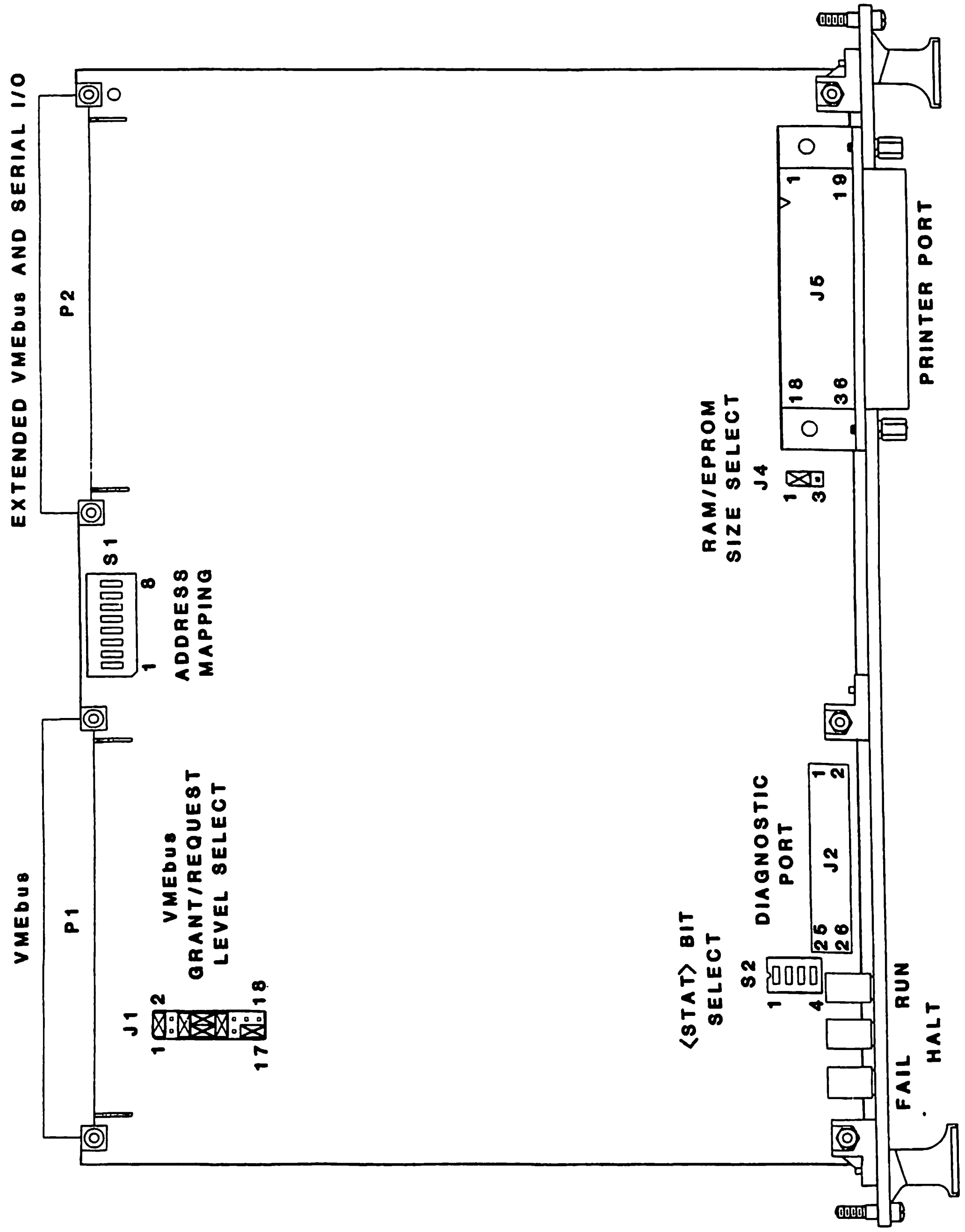
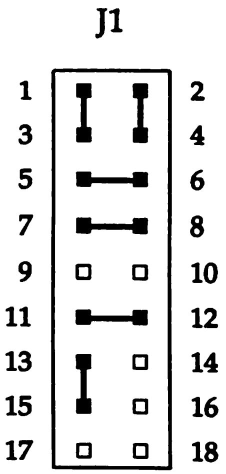


Figure 2-1. MVME332XT Header Locations

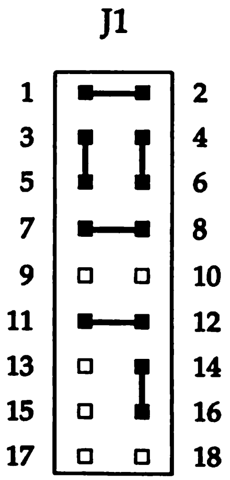
- Bus grant/request level select (J1)
- ROM/EPROM size select (J4)
- Address mapping switch (S1)
- <STAT> bit select switch (S4)

Bus Grant/Request Level Select Header (J1)

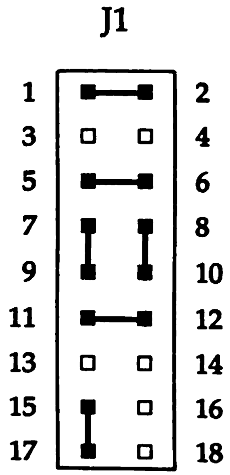
The VMEbus has four bus request levels (BR0* through BR3*), each having an associated bus grant (BG0IN*/BG0OUT* through BG3IN*/BG3OUT*) daisy-chain. Level 3 has the highest priority while level 0 has the lowest. Header J1 allows you to select the desired priority level for VMEbus accesses. The following illustrations show the proper configuration for each bus arbitration level. The module is shipped set for level 2.



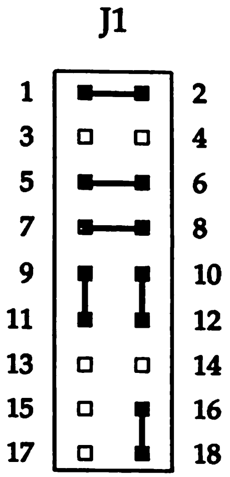
Bus Grant/Request Level 0



Bus Grant/Request Level 1



Bus Grant/Request Level 2



Bus Grant/Request Level 3

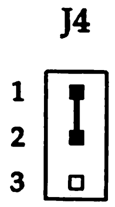
Suggestion: In SYSTEM V/68 configurations, the standard MVME332XT implementation does not utilize the VMEbus requester circuit, so to avoid BGIN-BGOUT daisy-chain delays (60 nanoseconds) for system slots occupied by multiple MVME332XTs, configure each MVME332XT at some bus request level not used by downstream VMEbus controllers. For example, if the disk controller and tape controller are at bus request levels 3 and 2 respectively, and are installed to the right of the MVME332XT(s), configure the MVME332XTs to level 0 or 1. This scheme causes no daisy-chain delay at slots occupied by MVME332XTs.

In single level arbiter systems; i.e., one request level, configure each MVME332XT at a different level from the rest of the system controllers.

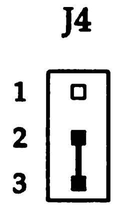
ROM/EPROM Size Select Header (J4)

Header J4 selects the size of ROMs/EPROMs used in sockets U57 and U60. The MVME332XT is factory configured with a jumper between pins 1 and 2 for 64K x 8 devices. If you are using 32K x 8 devices, set the jumper between pins 2 and 3.

The module is shipped configured for 64K x 8 devices.



64K x 8 Devices



32K x 8 Devices

Address Mapping Switch (S1)

Switch S1 maps the MVME332XT to any 64K byte boundary. The MVME332XT VMEbus port base address is selectable via the eight-position DIP switch (S1), which is located between the VMEbus connectors P1 and P2. The MVME332XT base address assignments and associated switch settings to be used with the MVME332XT SYSTEM V/68 driver are shown in the following tables.

NOTE

The module is delivered with a PAL at U20 that allows A32 addressing only. To allow the module to be used in A24 systems, a MVME332XT A32/A24 compatibility kit (part number 67-W2009C01) consisting of a replacement PAL for U20 must be used.

Table 2-1. MVME332XT Addressing for SYSTEM V/68 (A32 Systems)

Board Number	S1 Switch Positions 1	2	3	4	5	6	7	8	Base Address
0	ON	OFF	OFF	OFF	OFF	ON	ON	ON	FF780000
1	ON	OFF	OFF	OFF	OFF	ON	ON	OFF	FF790000
2	ON	OFF	OFF	OFF	OFF	ON	OFF	ON	FF7A0000
3	ON	OFF	OFF	OFF	OFF	ON	OFF	OFF	FF7B0000
4	ON	OFF	OFF	OFF	OFF	OFF	ON	ON	FF7C0000
5	ON	OFF	OFF	OFF	OFF	OFF	ON	OFF	FF7D0000
6	ON	OFF	OFF	OFF	OFF	OFF	OFF	ON	FF7E0000
7	ON	OFF	OFF	OFF	OFF	OFF	OFF	OFF	FF7F0000

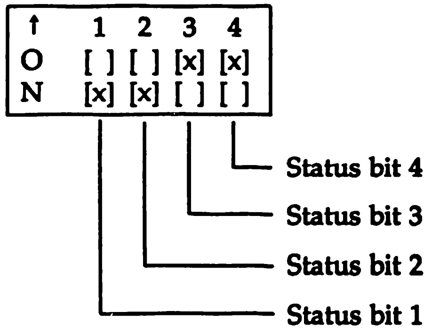
Table 2-2. MVME332XT Addressing for SYSTEM V/68 (A24 Systems)

Board Number	S1 Switch Positions 1	2	3	4	5	6	7	8	Base Address
0	OFF	OFF	OFF	ON	OFF	ON	ON	ON	E80000
1	OFF	OFF	OFF	ON	OFF	ON	ON	OFF	E90000
2	OFF	OFF	OFF	ON	OFF	ON	OFF	ON	EA0000
3	OFF	OFF	OFF	ON	OFF	ON	OFF	OFF	EB0000
4	OFF	OFF	OFF	ON	OFF	OFF	ON	ON	EC0000
5	OFF	OFF	OFF	ON	OFF	OFF	ON	OFF	ED0000
6	OFF	OFF	OFF	ON	OFF	OFF	OFF	ON	EF0000
7	OFF	OFF	OFF	ON	OFF	OFF	OFF	OFF	EF0000

<STAT> Bit Select Switch (S2)

The four-position DIP switch S2 on the MVME332XT is used to select the <STAT> bits **stat4-1** (located at onboard address $F90029). This is useful for conveying special board level configuration information to the MVME332XT debugger, diagnostic, and firmware. Switch S2 is located by the LED indicators and should be set as follows.

The module is shipped with switch S2 set as shown below. ON is 0, OFF is 1.



Derivative Systems

The MPU family MVME130, MVME131, MVME131XT, and the MVME132XT, which are all A24/32, D32/16 bus masters, is collectively referred to as MVME130 derivatives. Likewise, the MVME120, MVME121, MVME122, and MVME123 MPU family, which are A24/D16 bus masters, be referred to as MVME120 derivatives.

The MVME332XT slave interface is compatible with A32/24, D16 VMEbus masters, which implies that the addressing range is not an issue, but the data path with which it communicates with the MVME332XT must be D16, or 16 bits wide. If a D32 VMEbus reference is made to the MVME332XT, the module does not respond to the reference, causing the VMEbus system controller to issue the BERR* signal, which initiates bus error processing on the system MPU. In a typical operating system environment, bus errors on controller accesses often result in system crashes; i.e., type 2 panic traps.

The MVME332XT is not, by default, compatible with MVME120 derivative systems, and is compatible with MVME130 derivative systems if the PAL (Programmable Array Logic) device located at U46 on the MVME130 derivative is Motorola part number 51AW4591D27 or a later version. This PAL provides VMEbus data width decode on the MVME130 derivative, and designates the $F0000000 to $FFFFFFFF VMEbus space as D16. Without the aforementioned

PAL, longword (32-bit) references to a longword aligned VMEbus location in the $Fxxxxxxx address range causes the MVME130 derivative to issue the VMEbus LWORD* signal, indicating that the entire 32-bit VMEbus data path is valid for that reference. If the reference target is actually a D16 VMEbus device, such as the MVME332XT, the slave does not respond, causing a bus timeout.

With the 51AW4591D27 part installed, the MVME130 derivative actually executes the longword transfer to the $Fxxxxxxx VMEbus space by running two word size transfers; that is, the MVME130 derivative VMEbus interface breaks longword aligned, 32-bit references to VMEbus locations in the $Fxxxxxxx range into two 16-bit cycles by utilizing the MC68020 dynamic bus sizing control signals. With the 51AW4591D27 part installed, a 32-bit reference to a longword aligned VMEbus location in the $0 to $EFFFFFFF range results in one longword transfer attempt, consistent with VMEbus D32 operation.

Therefore, with the 51AW4591D27 part installed, D16 and D32 VMEbus slaves must be located in the following spaces:

MVME130 Derivative MPU, A32 Mode Data Width

VMEbus Address Range	VMEbus Data Width
$00000000 to $EFFFFFFF	D32 (32-bit data)
$F0000000 to $FFFFFFFF	D16 (16-bit data)

Installation Instructions

When the MVME332XT has been configured as you desire, install it in the system as follows:

1. Turn all equipment power OFF, and disconnect power cable from ac power source.

CAUTION

Connecting modules while power is applied may result in damage to components on the module.

WARNING

DANGEROUS VOLTAGES, CAPABLE OF CAUSING DEATH, ARE PRESENT IN THIS EQUIPMENT. USE EXTREME CAUTION WHEN HANDLING, TESTING, AND ADJUSTING.

2. Remove chassis cover as instructed in the equipment user's manual.
3. Remove the filler panel(s) from the appropriate card slot(s) at the front of the chassis. Refer to the *<STAT> Bit Select Switch (S2)* section in this chapter for proper setting.
4. Insert the MVME332XT into the selected card slot. Be sure the module is properly seated in the backplane connectors. Fasten the module in the chassis using the screws provided.
5. Make certain that the intended slot does not have VSB or VMX32 bus cabling on P2, because that could potentially damage the MVME332XT interface.
6. Connect the MVME710/MVME710A module as instructed in the MVME710/MVME710A user's manual.

7. At the MVME332XT slot on the backplane, remove the IACKIN*/IACKOUT* jumper and the BGIN*/BGOUT* jumper of the used priority level. Install BGIN*/BGOUT* jumpers on the unused levels.
8. Replace cover (if removed).
9. Turn equipment power ON.

CHAPTER 3
OPERATING INSTRUCTIONS

Introduction

This chapter provides necessary information to use the MVME332XT module in a system configuration. This includes indicators, and memory map details.

LED Indicators

The MVME332XT has three LED indicators (HALT, RUN, and FAIL) located on the front panel.

FAIL Indicator DS1

The red LED FAIL indicator, indicates the status of the fail bit in the control register.

HALT Indicator DS2

The red LED HALT indicator, is lit when the MC68010 microprocessor enters a halted state (usually the result of a double bus fault). The indicator is also lit whenever the MC68010 is being reset.

RUN Indicator DS3

The green LED RUN indicator, is connected to the MC68010 local data transfer acknowledge (DTACK*) and indicates that the MC68010 is completing a bus cycle. If the RUN LED is dim, the MVME332XT is relatively idle. When brightly illuminated or pulsing, the controller is active.

Local Address Map

The following table provides the general local address map for the MVME332XT.

Table 3-1. Local Address Map

Device	Local Address Range and Function Code	Comments
VMEbus window (MOVES access)	$0x000000 - 0xFFFFFF FC2-0 = 0 x x	VMEbus addr modifier sourced from <vam> register (16 Meg window)
VMEbus window (default mode)	$0x000000 - 0xEFFFFF FC2-0 = 1 x x	VMEbus addr modifier sourced from <vam> register (15 Meg window)
All onboard devices SIO devices, MC68230	$0xF00000 - 0xFFFFFF FC2-0 = 1 x x	See details below. (1 Meg Allocation)
196K local RAM	$0xF00000 - 0xF2FFFF FC2-0 = 1 x x	16-bit data path (196K allocation)
local port to 64K dual ported RAM	$0xF30000 - 0xF3FFFF FC2-0 = 1 x x	16-bit data path (64K allocation)
local RAM spare	$0xF40000 - 0xF7FFFF FC2-0 = 1 x x	access to this space may cause bus error (256K allocation)
MK68564 serial comm controllers	$0xF80000 - 0xF8FFFF FC2-0 = 1 x x	all four MK68564s on odd addresses (64K allocation)
local control/status registers	$0xF90000 - 0xF9FFFF FC2-0 = 1 x x	see local CSR section (64K allocation)
MC68230: timer, <vam> register, printer port	$0xFA0000 - 0xFAFFFF FC2-0 = 1 x x	occupies 64 locations on odd addresses (64K allocation)
unimplemented	$0xFB0000 - 0xFBFFFF FC2-0 = 1 x x	no local DTACK* for accesses to this space (64K allocation)
ROM space (up to 64K X 8 ROMs)	$0xFC0000 - 0xFDFFFF FC2-0 = 1 x x	32K x 8, 64K x 8 ROMs supported (128K allocation)
unimplemented	$0xFE0000 - 0xFFFFFF FC2-0 = 1 x x	access to this space may cause bus error (128K allocation)

Detailed Local Address Map

The following table provides the detailed local address map for the MVME332XT.

Table 3-2. Detailed Local Address Map

Address	Comments
F00000 - F0FFFF	Local RAM block 0, 64K bytes, 16-bit data.
F10000 - F1FFFF	Local RAM block 1, 64K bytes, 16-bit data.
F20000 - F2FFFF	Local RAM block 2, 64K bytes, 16-bit data.
F30000 - F3FFFF	Local port to 64K byte dual ported RAM, 16-bit data.
F40000 - F7FFFF	Local RAM expansion (unimplemented), may cause bus error.
F80000 - F81FFF	SIO #0 registers, 32 locations, odd addresses (serial ports 1 & 2).
F82000 - F83FFF	SIO #1 registers, 32 locations, odd addresses (serial ports 3 & 4).
F84000 - F85FFF	SIO #2 registers, 32 locations, odd addresses (serial ports 5 & 6).
F86000 - F87FFF	SIO #3 registers, 32 locations, odd addresses (serial ports 7 & 8).
F88000 - F89FFF	Diagnostic serial port, accessible via the diagnostic connector, 16 locations, odd addresses.
F8a000 - F8FFFF	Unimplemented, will cause bus error.
F90000 - F9001F	Unimplemented, may cause bus error.
F90020	Unimplemented, DTACK* returned.
F90021	<aux> local control register, read/write.
F90022	Unimplemented, DTACK* returned.
F90023	<vir> local control register, read/write.
F90024	Unimplemented, DTACK* returned.

Table 3-2. Detailed Local Address Map (cont'd)

Address	Comments
F90025	<vaer> local control register, write only.
F90026 - F90028	Unimplemented, DTACK* returned.
F90029	<stat> local status register, read/write (see note).
F9002A - F9002E	Unimplemented, DTACK* returned.
F9002F	Diagnostic display, accessible via the diagnostic connector, write only.
F90030 - F9FFFF	Unimplemented, will cause bus error.
FA0000 - FAFFFF	MC68230 PIT, 64 locations, odd addresses.
FB0000 - FBFFFF	Unimplemented, will cause bus error.
FC0000 - FDFFFF	ROM space, 32K and 64K by 8 devices supported.
FE0000 - FFFFFF	Unimplemented, may cause bus error.

NOTES: The local references shown in the table assume that the function code values are:

FC2-0 = 1 x x

which includes supervisor mode program and data cycles. Any MVME332XT processor cycle out of this function code range initiates a VMEbus request, regardless of address.

The status information contained in <stat> is available on read cycles to this location; writes to this location (with arbitrary data) clear the current bus error source status information in <stat>. Refer to the *Local Control/Status Register* section in Chapter 4 for more details.

CHAPTER 4
FUNCTIONAL DESCRIPTION

Introduction

This chapter describes the functions of the MVME332XT. The discussion includes local and dual access control/status information, local interrupts, and EIA-232-D signals supported by the MVME332XT controller and the MVME710/MVME710A transition modules. For the purpose of the following description, the MVME332XT is regarded as consisting of functional blocks as illustrated in Figure 4-1. For further details, refer to the *Related Documentation* section in Chapter 1.

Local Processor

The MVME332XT utilizes a 12.5 MHz MC68010 microprocessor, hereafter referred to as the MPU, as the MVME332XT engine. The MPU has access to all onboard resources such as control/status registers (both the local and VMEbus devices), ROM, local and dual ported RAM, MC68230 Parallel Interface and Timer, and all four MK68564 Serial I/O Controllers. The MPU also has access to the D16, A24/32 VMEbus interface via the VMEbus bus requester circuitry.

Other MVME332XT devices clocked at the MPU clock frequency include the VMEbus requester state machine and the local timeout circuitry.

ROM Space

The MVME332XT design accommodates 256K (32K x 8) and 512K (64K x 8) JEDEC standard 28-pin ROMs and/or EPROMs with access times in the 0 to 150 nanosecond range. Note that the MVME332XT design does not support devices out of the aforementioned speed and density ranges. The density selection (256K or 512K) is made through header J4. Refer to the *ROM/EPROM Size Select Header (J4)* section in Chapter 2.

Local RAM

The MVME332XT utilizes six 32K x 8 static RAMs, organized in three 32K 16-bit word blocks, to provide 196K of zero wait state local RAM. The MVME332XT functionality is only guaranteed with 28-pin, JEDEC standard pinout, 100 nanosecond access time (or less) 32K x 8 static RAMs installed in the static RAM sockets. No other part types should be installed at these locations. The MVME332XT hardware design does not support data parity or error correction for local or dual ported RAM accesses.

The MVME332XT firmware utilizes the local RAM for input and output character ring buffers, process stack area, vector tables, and downloadable line disciplines.

Serial Ports

The MVME332XT utilizes the MK68564 dual channel serial I/O controller to implement all eight serial ports. Note that only asynchronous serial I/O devices are supported. Each channel baud rate, when derived from the MVME332XT 2.4576 MHz baud rate clock, is selectable for 50 to 38.4K baud operation via the MK68564 time constant register. All serial I/O signals are accessible at the MVME332XT P2 connector and are compatible with the EIA-232-D standard (refer to the *MVME710 Table 4-2 or SIMVME710A* for signal descriptions). The following EIA-232-D signals are supported by the MVME332XT in conjunction with the MVME710/MVME710A transition modules.

Table 4-1. EIA-232-D Support by MVME332XT/MVME710/MVME710A

EIA-232-D Signal Name	DB-25 Connector	MVME710/MVME710A Configuration (Connect to Terminal)	MVME710/MVME710A Configuration (Connect to Modem)
PGND	1	Connected to MVME710/ MVME710A front panel (note 1)	Connected to MVME710/ MVME710A front panel (note 1)
TxD	2	Input	Output
RxD	3	Output	Input
RTS	4	Input	Output
CTS	5	Output	Input
DSR	6	Output	No DSR support by MVME332XT/VME710 in the Connect to Modem configuration (note 2)
SGND	7	Connected to module signal ground plane	Connected to module signal ground plane
DCD	8	Output	Input
TxC	15	Not supported	Not supported
RxC	17	Not supported	Not supported
DTR	20	Input	Output

NOTES: 1. To ensure proper connection between the EIS-232-D cable shield and the VME enclosure, you should utilize cables terminated with connectors that have the metal shell connected to the cable shield lead. The MVME710/MVME710A serial port connectors connect pin 1 to the VME system chassis ground via the MVME710/MVME710A front panel, but you are warned not to rely upon a connection between the cable shield lead and the cable DB-25 connector pin 1 for proper chassis ground connection. The chassis ground traces on the MVME710/MVME710A circuit board do not handle excessive currents (greater than .5A) flowing between each MVME710/MVME710A DB-25 connector and the chassis into which it is installed. Ground currents of considerable amplitude are common in remote computer/terminal/modem systems that connect associated equipment chassis grounds via shielded cables. Again, you should connect the EIA-232-D cable shield to the connector metal shell to ensure proper cable shielding when using the MVME332XT/MVME710 or MVME332XT/MVME710A module set.

Note that the MVME710/MVME710A front panel must make electrical contact with the VME system chassis ground (which ultimately should make electrical contact with the three wire ac line cord ground return) to ensure proper EMI shielding. Such a wiring scheme ensures a low resistance path for transient currents associated with accidental ac wiring faults and electrostatic discharges.

Also note that the PGND (chassis ground) signal is not connected to the cable between the MVME332XT and the MVME710/MVME710A, and is not connected to the SGND (signal ground) signal located at the DB-25 connector, pin 7.

2. The MK68564 does not have a DSR input, so the EIA-232-D DSR signal is not supported in the MVME710 "Connect to Modem" configuration. In the MVME710/MVME710A "Connect to Terminal" configuration, the DSR signal is sourced by the MK68564 DTR output signal. Refer to the *MVME710/MVME710A User's Manual* for more details.

Printer Port

The MVME332XT parallel printer port, accessible via the front panel mounted Centronics-compatible connector (J5), is implemented with the MC68230 PIT (Parallel Interface and Timer). The printer connector provides the 36 conductor Centronics interface, and is the EMI shielded type for reduced electrical interference outside the VME system enclosure. Note that the MVME332XT front panel must make electrical contact with the VME system chassis ground (which ultimately should make electrical contact with the three wire ac line cord ground return) to ensure proper EMI shielding.

The printer cable and connectors must be provided by the customer. The cable is 36 conductor, 26- or 28-AWG stranded, .050 inch conductor spacing flat ribbon cable, which should be compatible with the mass terminated connector type. The connector on the MVME332XT end of the cable is the 36-pin, mass terminated ribbon cable type, such as listed in the following table.

Table 4-2. Compatible Printer Cable Connectors

Vendor	Vendor Part Number
3M	3366-1001
T & B Ansley	622-36MAM

You should consult the Centronics compatible printer user's manual for the proper connector type for the printer end of the cable. Refer to *MVME710 Table 4-4 or SIMVME710A Support Information* for detailed descriptions of the MVME332XT J5 printer connector signals.

Local Interrupt Handler

The MVME332XT interrupt handler responds to local device interrupts and certain VMEbus events. The interrupt handler priority assignments and a description of the source of each interrupt are described in the following table. The MVME332XT architecture does not include a VMEbus interrupt handler. The VME system MPU must use the attention bit (located in the MVME332XT VMEbus <vcsr> CSR register file) to send interrupt type signals to the MVME332XT. Note that the local interrupt handler is disabled when the imsk local control bit is set (=1), which is the reset state. Refer to the *Control/Status Registers* section in this chapter for more details.

Table 4-3. Local Interrupt Handler

IRQ Level	Interrupt Source	Comments
7	ACFAIL* from VMEbus	Autovectored; nonclearable
6	SCCIRQ*; serial I/O interrupt from MK68564 communication controllers	MK68564s request interrupt service via SCCIRQ*. The MK68564s vector upon receipt of their IACK input.
5	TIRQ*; MC68230 timer interrupt	Firmware timeslice interrupt; autovectored.
4	PIRQ*; MC68230 printer port interrupt	Vectored from MC68230 during IACK cycle.
3	DIAGIRQ*; factory test support interrupt from diagnostic test adapter	Used only with test diagnostics; autovectored.
2	None	No interrupt at this level.
1	ATTNIRQ*; <vcsr> VME CSR attention bit	Indicates that another VMEbus device has set the MVME332XT <vcsr> VME CSR attention bit (attn); autovectored.

VMEbus Master Interface

The MVME332XT local MPU is able to initiate a decoded VMEbus request according to the MVME332XT Local Address Map in this manual. The MVME332XT VMEbus master interface is classified as a A32/24, D16 type, which means that the module is capable of addressing 32- or 24-bit VMEbus slaves over a 16-bit data path. The relevant VMEbus address space size; i.e., A32 or A24, is indicated by the VMEbus address modifier that the MVME332XT is sourcing for any particular VMEbus reference. Any MVME332XT firmware should write a valid A32/A24 address modifier into the <vam> local control register before referencing another VMEbus resource. Refer to the VMEbus specification for details regarding address modifier codes.

MVME332XT VMEbus master interface features include:

- A32/A24 VMEbus addressing, D16 data bus width. Read/Modify/Write cycles are supported for VMEbus references initiated by the MVME332XT. The master interface supports Read/Modify/Write cycles and the slave interface does not.
- VMEbus requester is Release on Request design that supports early release of BBSY*, and may be configured for fairness mode operation to reduce bus starvation problems in heavily loaded VME systems.
- VMEbus request timeout support allows a local bus error to terminate the onboard VMEbus request without violating any VMEbus bus request timing specifications. This allows time-critical firmware routines that access the VMEbus to abort a bus access within a programmable time interval, thereby avoiding character overruns.

Note that the current MVME332XT implementation does not utilize the VMEbus requester. The following discussion pertains to operation requiring the requester circuitry.

When the MVME332XT references a VME device, it must perform a VMEbus request, and then wait for the BGxIN* signal at the corresponding level. If the VME system is heavily loaded, the MVME332XT may have to wait an undesirable time interval before it is granted the VMEbus. To avoid this hangup condition, MVME332XT VMEbus requests are time constrained by timeout circuitry, which is programmable to allow various timeout intervals. If the MVME332XT requester receives its BGxIN* signal before the timeout event occurs, the timeout circuitry is reset, and the VMEbus cycle proceeds with the usual address/data strobes.

VMEbus Slave Interface and Decoding

The MVME332XT dual ported RAM space is available as a VMEbus slave to VMEbus cycles that satisfy the decoding conditions explained in this section. The MVME332XT VMEbus slave interface falls into the A32/A24, D16 category, which means that a slave request is issued to the dual port arbiter when:

1. The VMEbus reference is within the MVME332XT base address range, selectable via an eight position switch (S1). That is, VMEbus A23 to A16 match the switch S1 setting per the VMEbus Port Base Address Selection table in this section.

*** * * AND * * ***

2. The VMEbus LWORD* signal is negated.

*** * * AND * * ***

3. Either of the VMEbus data strobes DS1*, DS0* are asserted.

*** * * AND EITHER * * ***

4. The VMEbus reference is A32 mode; i.e., VMEbus AM5-0 = 0x0d or 0x0e, and VMEbus A31-A24 = 0xff.

*** * * OR * * ***

5. The VMEbus reference is A24 mode; i.e., VMEbus AM5-0 = 0x3d or 0x3e, in which case VMEbus A31 to A24 are irrelevant. Refer to the note on page2-6.

Read/Modify/Write cycles by another VMEbus master to the MVME332XT dual ported RAM are not supported. Any semaphore based resource allocation schemes must locate semaphores in VMEbus memory (other than the dual ported RAM that supports Read/Modify/Write cycles).

The MVME332XT slave decoder does not issue a slave port request for VMEbus short I/O accesses. Refer to the VMEbus specification for details regarding address modifier codes. Note that the <vcsr> VMEbus Control/Status Registers occupy the first sixteen locations of the dual ported RAM, and the <vect> VMEbus Interrupt Vector Registers occupy the last sixteen dual ported RAM locations, with one spare word entry. Refer to the *Control/Status Registers* and the *VMEbus Interrupt Vector Registers* <vect> sections in this chapter for more details.

The MVME332XT VMEbus port slave interface base address jk byte is selectable via the S1 eight-position DIP switch. The S1 switch positions correspond to VMEbus address signals according to the following table. Note that in A32 VMEbus mode, the MVME332XT slave decoder only issues a slave request to the dual port RAM when the VMEbus address lines A31-A24=0xff. In either A32 or A24 VMEbus mode, the VMEbus address lines must match the jk setting at the S1 DIP switch.

Table 4-4. VMEbus Slave Decoding

VMEbus Mode	VMEbus Address Range	VMEbus AM	Attributes
A32	`0xFFjk0000 - 0xFFjkFFFF`	`0x0D`	R/W, extended supervisor data, 16-bit data port
A32	`0xFFjk0000 - 0xFFjkFFFF`	`0x0E`	R/W, extended supervisor program, 16-bit data port
A24	`0xjk0000 - 0xjkFFFF`	`0x3D`	R/W, standard supervisor data, 16-bit data port
A24	`0xjk0000 - 0xjkFFFF`	`0x3E`	R/W, standard supervisor program, 16-bit data port

NOTE: Refer to the note on page 2-6 for A24 addressing information.

Table 4-5. VMEbus Port Base Address Selection

S1 Switch Position	Corresponding VMEbus Address Signal
1	A23
2	A22
3	A21
4	A20
5	A19
6	A18
7	A17
8	A16

When a S1 switch position is in the ON state, its corresponding VMEbus address line must be logical 0 before a match for that VMEbus address line occurs. Likewise, when a S1 switch position is in the OFF state, its corresponding

VMEbus address line must be logical 1 before a match for that VMEbus address line occurs. Refer to the following tables for MVME332XT base addressing assistance.

Table 4-6. VMEbus A32 Mode Base Addressing

VMEbus A32 Mode Address Modifier (note)								
S1 Switch Positions (jk)								VMEbus Port
1	2	3	4	5	6	7	8	Base Address
OFF	OFF	OFF	OFF	OFF	OFF	OFF	OFF	0xFFFF0000
OFF	ON	OFF	ON	OFF	ON	OFF	ON	0xFFAA0000
ON	OFF	ON	OFF	ON	OFF	ON	OFF	0xFF550000
ON	ON	ON	OFF	ON	ON	ON	ON	0xFF100000

NOTE: Refer to the VMEbus Slave Decoding table in this section.

Table 4-7. VMEbus A24 Mode Base Addressing

VMEbus A24 Mode Address Modifier (note)								
S1 Switch Positions (jk)								VMEbus Port
1	2	3	4	5	6	7	8	Base Address
OFF	OFF	OFF	OFF	OFF	OFF	OFF	OFF	0xFF0000
OFF	ON	OFF	ON	OFF	ON	OFF	ON	0xAA0000
ON	OFF	ON	OFF	ON	OFF	ON	OFF	0x550000
ON	ON	ON	OFF	ON	ON	ON	ON	0x100000

NOTES: Refer to the VMEbus Slave Decoding table in this section.
Refer to note on page 2-6 for A24 addressing information.

Control/Status Registers

The MVME332XT architecture includes local and dual ported CSR (Control/Status Register) resources. The local CSR devices are accessible only by the MVME332XT MPU, but the dual ported registers are accessible by either the local MPU or by another VMEbus master, subject to conditions described in this section. The local MPU has access to all CSR registers, local and dual ported. Slave accesses via VMEbus references are supported only for the <vect> and <vcsr> dual ported registers.

The CSR devices include the VMEbus address extension register <vaer>, the VMEbus address modifier register <vam>, the VMEbus interrupter register <vir>, the auxiliary control register <aux>, the VMEbus interrupt vector registers <vect>, and the VMEbus CSR <vcsr>. The latter two devices, <vect> and <vcsr>, are dual ported register files located within the MVME332XT 64K dual ported RAM.

Auxiliary Control Register <aux>

D07	D06	D05	D04	D03	D02	D01	D00
disattn	ronr*	reserved	txoff	time	reserved	imsk	bdfail

Local Address: **$0xF90021**

Attributes: R/W, local only

disattn: disable attention bit control. Reset state: 1.

> The MVME332XT firmware can extinguish the attention bit interrupt (ATTNIRQ*) issued by another VMEbus master by clearing this bit location. The disattn bit resets to 1, disabling the ATTNIRQ* interrupt when the attn <vicr> VME csr control bit has been set.

ronr*: VMEbus requester fairness mode. Reset state: 1.

> The MVME332XT VMEbus requester may be configured for "request on no request" operation (ronr* = 0), in which the MVME332XT does not issue its VMEbus request until there are no bus requests present at the same level. In other words, if the MVME332XT is configured to generate VMEbus requests at level 3 in fairness mode (ronr* = 0) and has a pending VMEbus request but another VMEbus master already has a level 3 bus request asserted on VME, the MVME332XT waits until the current level 3 bus request has negated before it issues its level 3 bus request. Note that the reset state is the non-fairness mode (ronr* = 1).

txoff: serial port transmitter control. Reset state: 1.

The txoff control bit is useful primarily for diagnostics firmware support. If the txoff bit = 1, all eight serial port transmit lines will be disabled, allowing serial port local loopback testing to be performed without sending an entire sequence of control/escape characters to the console (which causes most terminals to undergo harmless but stressful gymnastics). The MVME332XT firmware must clear this bit (txoff = 0) before any attempt is made to communicate with any serial equipment connected to the MVME332XT serial ports.

time: VMEbus bus requester timeout select. Reset state: 1.

These bits are used to select the MVME332XT timeout interval for both onboard and VMEbus references. When the MVME332XT local data strobes assert, the timeout counter starts. If the timeout value specified by "time" expires before the appropriate signal is received (DTACK* for local cycles, bus grant in for VME cycles), the timing chain issues the local CPUBERR* signal to the MVME332XT MPU, and the <stat> register logs the event if the timeout resulted during a VME reference (the VMEto status bit is set in this case).

When the MVME332XT references a VME device, it must perform a VMEbus request, and then wait for the BGxIN* signal at the corresponding level. If the VME system is heavily loaded, the MVME332XT may have to wait an undesirable time interval before it is granted the VMEbus. To avoid this hangup condition, MVME332XT VMEbus requests are time constrained by timeout circuitry, which is programmable to allow various timeout intervals. If the MVME332XT requester receives its BGxIN* signal before the timeout event occurs, the timeout circuitry is reset, and the VMEbus cycle proceeds with the usual address/data strobes.

The following timeout intervals (local and VME) are supported:

Table 4-8. Timeout Control Bits

Time	Resultant Timeout Interval
0	Infinite; disable timeout.
1	20 microseconds, reset state.

imsk: local interrupt mask bit. Reset state: 1.

When imsk = 1, all local interrupts are disabled; that is, the MVME332XT MPU does not receive interrupts, allowing uninterrupted vector table initialization. When imsk = 0, all interrupts are enabled to the MVME332XT MPU.

bdfail: MVME332XT board level failure control bit. Reset state: 1.

If an unrecoverable error occurs on the MVME332XT, the firmware should write a 1 to the bdfail local CSR bit, which lights the fail LED and generate the VMEbus SYSFAIL* signal (provided that the sysfi VME <vcsr> control bit is cleared). The SYSFAIL* event typically generates an interrupt to the system MPU. The device driver may then issue a reset to the VME device (the MVME332XT may be reset by writing a 1 to the VMEbus <vcsr> reset control register bit) or decide to only respond to the SYSFAIL* event by extinguishing the SYSFAIL* signal, which may be accomplished by writing a 1 to the sysfi bit.

VMEbus Interrupter Register <vir>

D07	D06	D05	D04	D03	D02	D01	D00
**	**	**	**	**	vir2	vir1	vir0

** Denotes nonimplemented bit locations.

Local Address: $0xF90023

Attributes: R/W, local only

vir2-0: VMEbus interrupt level. Reset state: 000.

Any <vir> bit pattern other than 000 issues a VMEbus interrupt request per the following table. When the associated VMEbus interrupt request has been acknowledged, the <vir> bit field is automatically returned to the no-interrupt state, which is 000. The MVME332XT firmware should write the encoded interrupt request level to this field to generate a VMEbus interrupt request, as follows:

Table 4-9. VMEbus Interrupter Control Bits

VMEbus Interrupt Level	<vir2-0> Control
7	1 1 1
6	1 1 0
5	1 0 1
4	1 0 0
3	0 1 1
2	0 1 0
1	0 0 1
no interrupt	0 0 0

VMEbus Address Extension Register <vaer>

D07	D06	D05	D04	D03	D02	D01	D00
VME31	VME30	VME29	VME28	VME27	VME26	VME25	VME24

Local Address: **$0xF90025**

Attributes: Write only, local only

<vaer> is the VMEbus address extension register, used primarily for providing the upper eight address lines required for A32 VMEbus operation. When the MVME332XT references 24-bit address VME slaves, the VME address lines A31 through A24 are irrelevant, but the contents of the <vaer> register is still sourced to the VME A31-24 address lines when the MVME332XT has acquired VMEbus mastership. Note that when the MVME332XT references a 24-bit address slave, the contents of the <vaer> register is still sourced to the VME A31-24 address bits, but A24 slaves only decode VME A23-01 when the MVME332XT drives a valid A24 address modifier). In VME A32 mode, the VME A31-24 address lines are sourced from the <vaer> register when the MVME332XT has been granted bus mastership. Read attempts from the <vaer> register location are acknowledged, but the data returned from such a transfer is meaningless; i.e., reads from <vaer> does not result in a bus error). Reset state: 0x00.

VMEbus Address Modifier Register <vam>

D07	D06	D05	D04	D03	D02	D01	D00
&&	&&	vam5	vam4	vam3	vam2	vam1	vam0

&& Denotes implemented but reserved bit location.

Local Address: **$0xFA0013**

Attributes: R/W, local only

<vam> is the VMEbus address modifier register, which is sourced to the VMEbus along with address lines A31-01 after the MVME332XT has acquired VMEbus mastership. Note that the MVME332XT MPU function code signals FC2-0 are not used to generate the VMEbus address modifiers AM5-0. Reset state: <vam> = 0xFF.

<vam> is implemented with the MC68230 port B data register, located at 0xFA0013 in the local MVME332XT memory map. Reset state: unchanged by reset condition; however, this port is configured as an input port after reset. After reset, the firmware should initialize the port B data register to a known state and enable it as an output port via the Port General Control Register and the Port B Control Register (locations 0xFA0001 and 0xFA000f, respectively).

Local Status Register <stat>

D07	D06	D05	D04	D03	D02	D01	D00
stat4	stat3	stat2	stat1	**	locto	VMEberr	VMEto

** Denotes nonimplemented location.

Local Address: **$0xF90029**

Attributes: Partially R/W, local only

<stat> contains the bus error status bits locto, VMEberr, and VMEto which are the local timeout, VMEbus bus error, and VMEbus requester timeout status flags, respectively. <stat> also includes four switch selectable status bits, stat4-1 which are useful for conveying special board level configuration to the MVME332XT firmware; i.e., default baud rate, etc. Note that the only the locto, VMEberr, and VMEto status flags clear to 0 after a write cycle (with arbitrary data) to location 0xF90029. The state of the three bus error status flags is not guaranteed after

reset; therefore, MVME332XT firmware, diagnostics, and debuggers should perform a write cycle (data is arbitrary) to the <stat> location (0xF90029) soon after the reset vector fetch completes, thereby initializing the bus error status flags to the 0 0 0 state.

The suggested <stat> initialization procedure in assembly is:

```
                clr.b $F90029        clear bus error status bits
```

writes 0x00 to the <stat> location, clearing the bus error status flags. The bus error status flags cannot be cleared individually. The stat4-1 bits cannot be reset, and always indicate the S2 four-position DIP switch settings. Note that reads from <stat> have no effect on the bus error status flag state.

stat4-1: switch selectable status bits

> stat4-1 simply indicate the state of S2 settings, according to the following discussion. They are useful for conveying configuration information to the MVME332XT debugger, diagnostics, and firmware. Note that stat4-1 are read only, and are not affected by MVME332XT board level reset or writes to the <stat> location. Also note that there exists a one-to-one relationship between individual S2 switch positions 4, 3, 2, and 1 and the stat4-1 status register bits. If S2-4 is ON, a local read of <stat> returns a logical 1 for the stat4 status bit. Likewise, if S2-1 is OFF, a local read of <stat> returns a logical 0 for the stat1 status bit.

locto: local timeout

> If a local reference to a nondecoded local address is attempted, the cycle times out when the time interval specified by the time control bit has elapsed. When a local timeout occurs, the cycle terminates, the locto status flag is set to 1, and local bus error processing is performed. A local write to location 0xF90029 (with arbitrary data) clears the locto status flag, as well as the VMEberr and VMEto status flags. Note that all bus error status flags are cleared on a write cycle to location 0xF90029, whether any or all of them are set.

VMEberr: VMEbus bus error

> If a VMEbus slave issues the BERR* signal in response to an MVME332XT VMEbus reference, the cycle terminates, the VMEberr status flag is set to 1, and local bus error processing is performed by the MVME332XT firmware. That is, only VMEbus bus error events caused by MVME332XT references set the VMEberr flag. A local write to location 0xF90029 clears the VMEto flag to 0 (as well as the VMEberr and the locto status flags).

VMEto: VMEbus requester timeout

> If the MVME332XT VMEbus requester does not receive the BGxIN* bus grant signal within the time interval specified by the time control bit, the cycle terminates locally, the VMEto status flag is set to 1, and local bus error processing is performed. A local write to location 0xF90029 clears the VMEto flag to 0 (as well as the VMEberr and the locto status flags).

VMEbus Interrupt Vector Registers <vect>

Table 4-10. VMEbus Interrupt Vector Register File

Port	Address Range	Attributes
local	`0xF3fff0 - F3FFFE`	R/W, 16-bit data
A32 VMEbus	`0xFFjkFFF0 - FFjkFFFE`	R/W, 16-bit data
A24 VMEbus	`0xjkFFF0 - jkFFFE`	R/W, 16-bit data

NOTE: Refer to the note on page 2-6 for A24 addressing information.

<vect> is the VMEbus interrupt vector register file. Before the MVME332XT firmware issues a VMEbus interrupt request via the <vir> control register bits, the VMEbus interrupt vector that corresponds to the interrupt level must be written to this register file. During the subsequent interrupt acknowledge cycle, the MVME332XT hardware enables the vector associated with the current interrupt level to the VMEbus data bus followed by DTACK*, which terminates the VMEbus IACK cycle. The <vect> VME port base address jk byte is selectable for A32 or A24 slave accesses via switch S1 that is used to set the MVME332XT dual ported RAM base address. Note that each <vect> entry can be read or written to by the local MPU or by a VMEbus slave whose cycle satisfies the conditions specified in the *VMEbus Slave Interface and Decoding* section in this chapter. This means that switch S1 only sets the dual ported RAM VMEbus port base address. During VMEbus IACK cycles, the IACK level, indicated by the VMEbus A03-A01, is used to index into the last sixteen entries of the dual ported RAM for vector delivery (note that IACK level 0 entry is a reserved location).

The MVME332XT hardware ensures that a unique <vect> location is sourced per VMEbus interrupt level, allowing you supply the system MPU a unique vector for every possible VMEbus interrupt request level. Refer to the following table to correlate VMEbus interrupt request levels with associated VMEbus interrupt vectors, which are located in the MVME332XT dual ported RAM. The MVME332XT drives the VMEbus data paths D15-D00 or D07-D00 during VME

IACK cycles, depending upon which of the VME data strobes are asserted. Refer to the following table. The 16-bit addresses under the VME D15-D08 and VME D07-D00 table headings assume the offsets shown in the <vect> Register File table.

Table 4-11. VMEbus Interrupt Vectors

VMEbus Interrupt Vector Location as Function of VMEbus Data Strobes				
VMEbus LWORD* = 1			**VMEbus IACK Vector Location from Dual Ported RAM**	
VMEbus IACK Level	**VME Data Strobes**			
	DS1*	**DS0***	**VME D15-D08**	**VME D07-D00**
no IRQ	X	X	Reserved	Reserved
1	0 0 1	0 1 0	FFF2 FFF2 not valid	FFF3 not valid FFF3 (note)
2	0 0 1	0 1 0	FFF4 FFF4 not valid	FFF5 not valid FFF5 (note)
3	0 0 1	0 1 0	FFF6 FFF6 not valid	FFF7 not valid FFF7 (note)
4	0 0 1	0 1 0	FFF8 FFF8 not valid	FFF9 not valid FFF9 (note)
5	0 0 1	0 1 0	FFFA FFFA not valid	FFFB not valid FFFB (note)
6	0 0 1	0 1 0	FFFC FFFC not valid	FFFD not valid FFFD (note)
7	0 0 1	0 1 0	FFFE FFFE not valid	FFFF not valid FFFF (note)

NOTE: Motorola VMEbus MPU products typically support this type of IACK cycle.

Dual Port Arbiter

The MVME332XT dual port arbiter accepts asynchronous dual ported RAM requests from the VMEbus slave decoding circuit (SLVREQ*) and from the local decoding circuit (LDPREQ*) and issues the appropriate local (LGNT*) or slave (SGNT*) grant signal, depending upon the outcome of the arbitration. In case of simultaneous requests, the slave port is granted the dual ported RAM address and data bus. At the end of either a slave or local cycle, the dual port arbiter is cleared, ready for the next request. The dual ported bus is granted to either the slave or local ports on a cycle by cycle basis.

Dual Port RAM

The MVME332XT utilizes two 32K x 8 static RAMs, organized as one 32K 16-bit word block, to provide a 64K dual ported RAM resource. The MVME332XT functionality is only guaranteed with 28-pin, JEDEC standard pinout, 100 nanosecond access time (or less) 32K x 8 static RAMs installed in the static RAM sockets. No other part types should be installed at these locations. The MVME332XT hardware design does not support any error correction schemes for local or slave dual ported RAM accesses. Read/Modify/Write accesses to the dual ported RAM by another VMEbus master are not fully supported.

The MVME332XT firmware utilizes the dual ported RAM for read and write ring character buffers and for the Buffered Pipe Protocol channel structures. By locating these data structures in dual ported RAM, the MVME332XT firmware interrupt handler does not have to issue VMEbus requests to transfer characters or access its command/status channel, which directly reduces the MVME332XT VMEbus bandwidth requirements and ensures that the firmware character I/O routines are deterministic in nature.

Refer to the *Local Address Map* section in Chapter 3 for the dual ported RAM local port base address. You are referred to the *VMEbus Slave Interface and Decoding* section in this chapter for the dual ported RAM slave access considerations.

Note that the <vcsr> VMEbus Control/Status Registers occupy the first sixteen locations of the dual ported RAM, and the <vect> VMEbus Interrupt Vector Registers occupy the last sixteen dual ported RAM locations. Refer to the *Control/Status Registers* section and the <vect> *VMEbus Interrupt Vector Registers <vect>* table in this chapter for more details.

Table 4-12. MVME332XT Dual Port RAM Map

Addresses: A32 Slave Port (Local Port)	Dual Port RAM Upper Byte 15 8	Dual Port RAM Lower Byte 7 0
0xFFjk0000 (0xF30000) 0xFFjk000E (0xF3000E)	<vcsr> IPC Control/Status Registers	
0xFFjk0010 (0xF30010) 0xFFjkFFEE (0xF3FFEE)	RAM available for IPC channel structures and character read/write ring buffers	
0xFFjkFFF0 (0xF3FFF0) 0xFFjkFFFE (0xF3FFFE)	<vect> VMEbus Interrupt Vector Registers	

The dual ported RAM base address jk byte is selectable for A32 or A24 VMEbus cycles via switch S1. Note that S1 setting does not affect the dual ported RAM local port base address.

VMEbus Control/Status Registers <vcsr>

Table 4-13. VMEbus Dual Ported Control/Status Register File

Port	Address Range	Attributes
A32 VMEbus	0xFFjk0000 - 0xFFjk000F	R/W, 16-bit data
A24 VMEbus	0xjk0000 - 0xjk000F	R/W, 16-bit data
local	0xF30000 - 0xF3000F	R/W, 16-bit data

NOTE: Refer to the note on page 2-6 for A24 addressing information.

The <vcsr> is a dual ported R/W register file that occupies the first 16 locations of the MVME332XT 64K dual ported RAM space. Each port address range is given in the table above, and specific locations are shown in the register map in the following table. The address associated with each <vcsr> entry is shown to the left of the register map. The local address is in parenthesis; the other is the corresponding A32 mode VMEbus location.

The <vcsr> VME port base address jk byte is selectable via switch S1. The VME port addresses shown in the map below are relevant for A32 VME operation. The corresponding A24 addresses are obtained by simply deleting the leading 0xFF upper byte of the A32 VME 24-bit address local memory map. The local port resides in the MVME332XT 24-bit local memory map. Locations denoted available are undefined R/W entries that are available for your definition. Those marked reserved are implemented register locations that are defined for future expansion; that is, you are cautioned not to use these locations. Locations marked n/i are physically nonimplemented; that is, reads return a logical 1 for the associated data bits, and writes are not supported.

Table 4-14. VMEbus Dual Ported CSR File Map

<table>
<tr><th>Addresses:
A32 VME
(Local)</th><th colspan="2">Dual Port RAM
Upper Byte
15 8</th><th>Dual Port RAM
Lower Byte
7 0</th></tr>
<tr><td>0xFFjk0000
(0xF30000)</td><td colspan="3">IPC Address Register (msw)</td></tr>
<tr><td>0xFFjk0002
(0xF30002)</td><td colspan="3">IPC Address Register (lsw)</td></tr>
<tr><td>0xFFjk0004
(0xF30004)</td><td colspan="2">IPC Address
Modifier Register</td><td>available</td></tr>
<tr><td>0xFFjk0006
(0xF30006)</td><td><vicr>
Control</td><td>n/i</td><td>reserved</td></tr>
<tr><td>0xFFjk0008
(0xF30008)</td><td colspan="2">IPC Status
Register</td><td>reserved</td></tr>
<tr><td>0xFFjk000A
(0xF3000A)</td><td colspan="2">IPC Model
Register</td><td>reserved</td></tr>
<tr><td>0xFFjk000C
(0xF3000C)</td><td colspan="2">IPC Abort
Vector Register</td><td>available</td></tr>
<tr><td>0xFFjk000E
(0xF3000E)</td><td colspan="3">TAS Register</td></tr>
</table>

Refer to the *MVME332XTFW IPC Firmware User's Guide* for specific application details of the <vcsr> data structure.

VMEbus IPC Control Register <vicr>

Table 4-15. VMEbus IPC Control Register File

Port	Address	Attributes
A32 VMEbus	0xFFjk0006	R/W, only D15-D12 data bits implemented.
A24 VMEbus	0xjk0006	R/W, only D15-D12 data bits implemented.
local	0xF30006	R/W, only D15-D12 data bits implemented.

Table 4-16. VMEbus IPC Control Register <vicr>

D15	D14	D13	D12	D11	D10	D9	D8
busy	reset	attn	sysfi	n/i	n/i	n/i	n/i

busy: VMEbus CSR semaphore bit, active high, local and VMEbus R/W.

The MVME332XT may hold off the system MPU by setting this bit location, which occurs automatically upon reset. When the MVME332XT has performed sufficient housekeeping to accept commands from the host, the firmware should clear this bit, indicating a nonbusy state. Reset state: 1.

reset: reset bit, active high, local and VMEbus R/W.

The VMEbus reset control bit generates a complete hardware/software reset on the MVME332XT when the system MPU writes a 1 to this bit location. The reset bit implements a reset and hold function; that is, when reset = 1, the MVME332XT is held in the reset state until the VME system MPU writes a 0 to this bit location or until the VMEbus SYSRESET* signal is asserted. The MVME332XT reset state generated by the reset control bit is not automatically cleared by MVME332XT circuitry. Reset state: 0.

attn: attention bit, active high, local and VMEbus R/W.

The system MPU may generate a local interrupt on the MVME332XT by writing a 1 to the attn bit location, which is cleared when the MVME332XT responds to the interrupt. The system MPU should use the attn bit to signal the MVME332XT that a new command has been sent. Reset state: 0.

sysfi: VMEbus SYSFAIL* inhibit, active high, local and VMEbus R/W.

If an unrecoverable error occurs on the MVME332XT, the firmware should write a 1 to the bdfail local CSR bit, which lights the fail LED and generates the VMEbus SYSFAIL* signal. The SYSFAIL* event typically generates an interrupt to the system MPU, which determines which VME device has the failure condition. The driver may then issue a reset to the VME device (the MVME332XT may be reset by writing a 1 to the VMEbus reset control register bit) or decide to only respond to the SYSFAIL* event by extinguishing the SYSFAIL* signal, which may be accomplished by writing a 1 to the sysfi bit. Reset condition: 0, which connects the MVME332XT bdfail control bit (which resets to 1, asserted) to the VME SYSFAIL* signal. Therefore, after reset, the MVME332XT asserts its bdfail control bit, which generates the SYSFAIL* signal to the VME system MPU. The MPU can either ignore the SYSFAIL* signal, extinguish it by writing a 1 to the sysfi bit, or just wait until the MVME332XT completes its onboard confidence test, at which time the MVME332XT firmware negates its bdfail control bit.

Timer

The MVME332XT utilizes the MC68230 internal timer for firmware process periodic activation. The MC68230 is clocked at 2 MHz.

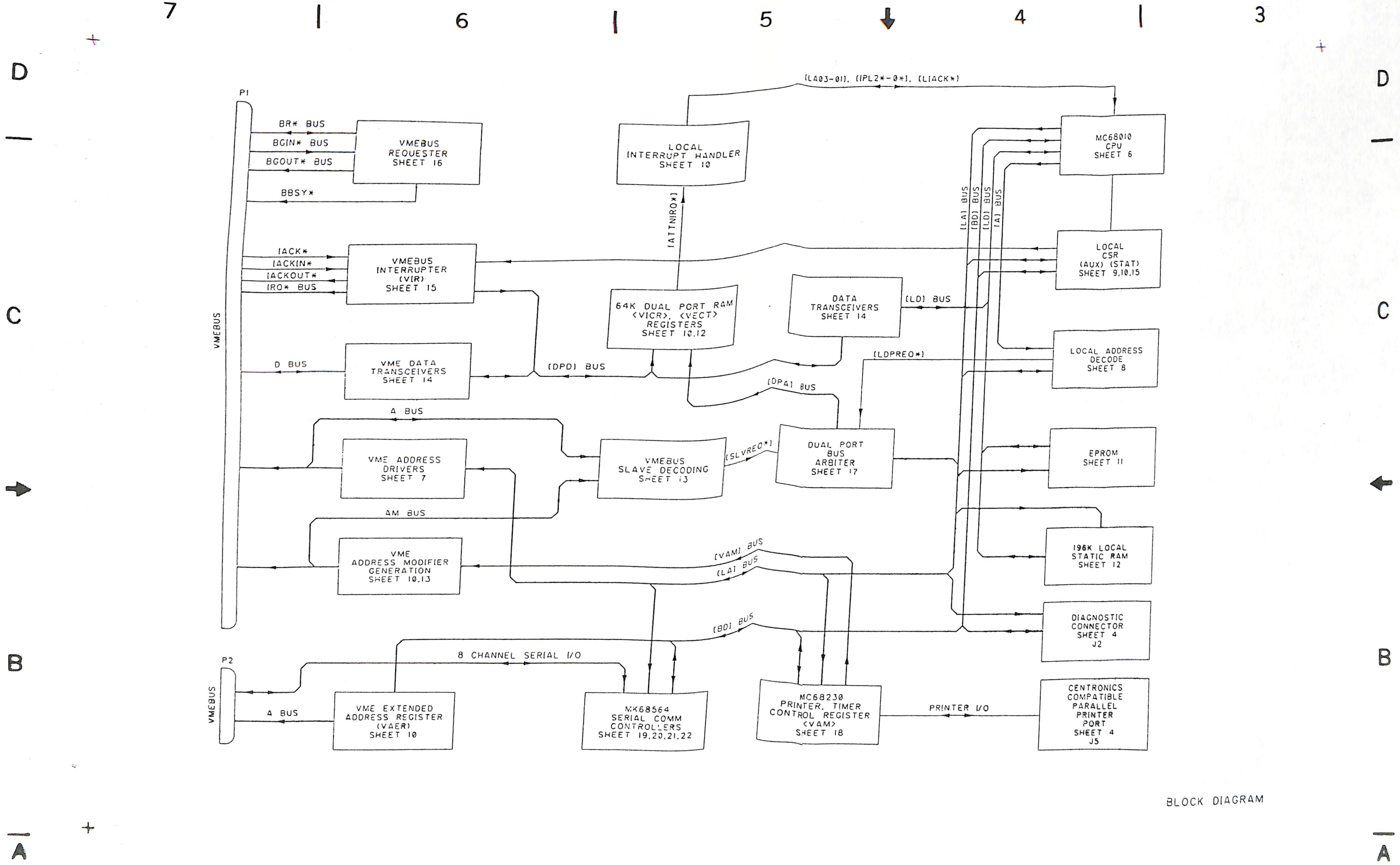

7
6
5
4
3
D
C
B
A
[LA03-01], [IPL2*-0*], [LIACK*]
P1
VMEBUS
BR* BUS
BGIN* BUS
BGOUT* BUS
BBSY*
VMEBUS REQUESTER SHEET 16
LOCAL INTERRUPT HANDLER SHEET 10
MC68010 CPU SHEET 6
[LA] BUS
[BD] BUS
[LD] BUS
[A] BUS
[ATTNIRQ*]
IACK*
IACKIN*
IACKOUT*
IRQ* BUS
VMEBUS INTERRUPTER (VIR) SHEET 15
LOCAL CSR (AUX) (STAT) SHEET 9,10,15
64K DUAL PORT RAM <VICR>, <VECT> REGISTERS SHEET 10,12
DATA TRANSCEIVERS SHEET 14
[LD] BUS
D BUS
VME DATA TRANSCEIVERS SHEET 14
[DPD] BUS
[LDPREQ*]
LOCAL ADDRESS DECODE SHEET 8
[DPA] BUS
A BUS
VME ADDRESS DRIVERS SHEET 7
VMEBUS SLAVE DECODING SHEET 13
[SLVREQ*]
DUAL PORT BUS ARBITER SHEET 17
EPROM SHEET 11
AM BUS
VME ADDRESS MODIFIER GENERATION SHEET 10,13
[VAM] BUS
[LA] BUS
196K LOCAL STATIC RAM SHEET 12
[BD] BUS
DIAGNOSTIC CONNECTOR SHEET 4 J2
8 CHANNEL SERIAL I/O
P2
VMEBUS
A BUS
VME EXTENDED ADDRESS REGISTER (VAER) SHEET 10
MK68564 SERIAL COMM CONTROLLERS SHEET 19,20,21,22
MC68230 PRINTER, TIMER CONTROL REGISTER <VAM> SHEET 18
PRINTER I/O
CENTRONICS COMPATIBLE PARALLEL PRINTER PORT SHEET 4 J5
BLOCK DIAGRAM

Figure 4-1. MVME332XT Block Diagram

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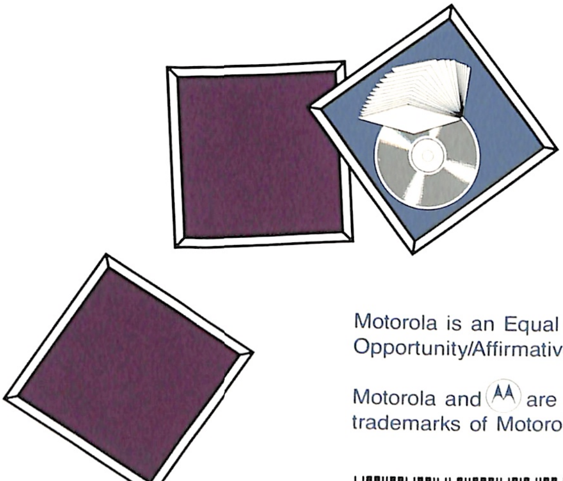

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