MVME166 VSB SPECIFIC ERRATA

The following errata are applicable to the MVME166 with VSBChip2 version 1. The version number of the VSBChip2 should be checked by reading the EVSB Attention Register to get the chip version value. The next revision of the chip will be version 2.

1) ERRATA: VSB Slave-to-Local bus Read Operation Size

Description: Read operations through the VSB slave to local master are not aligned properly when the programmed size (D08, D16 or D32) does not exactly match the size of the read operation (SINGLE_BYTE, DOUBLE_BYTE, or QUAD_BYTE respectively). Write operations are not affected.

Work-Around: A PAL fix has been implemented to force all VSB single-byte and double-byte read cycles to appear to the VSBchip2 as quad-byte read requests. This fix limits VSB slave block transfer support to 32-bit only.

2) ERRATA: Local-to-VSB Read Operation Size

Description: Read operations through the local bus to VSB are not aligned properly when the requested size is single-byte or double-byte. For single-byte transfers, the VSBchip2 always grabs the data from VSB data lines D31-D24. For double-byte transfers, the VSBchip2 always grabs the data from VSB data lines D31-D16. Write operations are not affected.

Work-Around: A PAL fix has been implemented to force all local bus single-byte and double-byte read cycles to appear to the VSBchip2 as quad-byte read requests. The 68040 MPU will correctly latch only the necessary data.

3) ERRATA: VSB Slave-to-Local Write Post Not Supported

Description: Write-posting through the VSB slave to local master causes erroneous memory locations to be altered. Also, write-posted data written through the VSB slave to local master interface is not properly aligned by the VSBchip2.

Work-Around: Do not enable VSB-slave write-posting: The WPE bit in both Slave Attribute Registers must be cleared.

4) ERRATA: Local-to-VSB Write Post Not Supported

Description: The local slave to VSB master interface fails when write posting is enabled and read-line transfers (cache load or MOVE16 instructions) are performed.

Work-Around: Disable the write-posting by clearing the WPE bit in all four Master Attribute Registers.

5) ERRATA: VSB Triple-Byte Operation Not Supported

Description: The VSB slave to local master interface does not properly handle triple-byte VSB accesses.

Work-Around: NONE

6) ERRATA: Un-aligned VSB Operation Not Supported

Description: The VSB slave to local master interface does not properly handle unaligned VSB accesses

Work-Around: NONE

7) ERRATA: Release-On-Request Mode Not Supported

Description: Release-On-Request (ROR) mode does not work with VSBchip2 version 1.

Work-Around: VSBchip2 must programmed to Release-When-Done (RWD) mode: The LVRWD bit in the VSB Requester Control/Status register must always be set.

8) ERRATA: VSB Slave Error Status Bits Not Properly Set

Description: Error Status bits (LBTE, LBPE, LBXE, and LBE) in the VSB Error Status Register are not set properly. When the VSBChip2 is functioning as the local bus master and receives a transfer-error-acknowledge (TEA* asserted and TA* negated), one of the 4 status bits is supposed to be set according to the value encoded on the Local bus status lines LST1-LST0. The encoding is as follows:

LST1	LST0	Status Bit Set
0	0	LBTE - Local Bus Timeout Error
0	1	LBXE - Local Bus Offboard Error
1	0	LBPE - Local Bus DRAM Parity/ECC Error
1	1	LBE - Local Bus Error

The problem is the value on LST1-LST0 is not latched into the register until the clock after TEA* is detected as low, which means the slave is no longer driving its error condition on LST1-LST0. Since the non-driven state of LST1-LST0 is %11, this is the value that is always being latched into the VSB Error Status Register.

Work-Around: LBE will always be the status bit set whenever a TEA* is returned. The VSBchip2 is correctly recording that an error occurred on the local bus (the slave has asserted TEA* in response to the transfer). Treat the LBE bit as a general bus error flag which encompasses all the above possible error sources.

9) ERRATA: Data Broadcall Not Supported by VSB Slave Interface

Description: Data Broadcall (participate-on-read mode) does not work reliably.

Work-Around: NONE

10) ERRATA: Participating Slave Mode Not Supported by VSB Slave #2

Description: VSB Slave #2 is unable to participate in either data broadcast or data broadcall operations.

Work-Around: Use VSB Slave #1 for data broadcast function.

11) ERRATA: Unlocked VSB Transfer May be Treated as Locked Bus Cycle

Description: An unlocked VSB slave-to-local master locked transfer immediately following a locked transfer may be mistakenly treated as a locked transfer. This problem does not apply to locked cycles performed by setting the software lock bits in the VSB Slave Attribute Registers.

Work-Around: NONE. This only affects the performance of the local bus under locked conditions.

12) ERRATA: Parallel Arbitration Mode Not Supported

Description: Parallel arbitration mode is not currently supported.

Work-Around: NONE